

**FIG. 1** (PRIOR ART)

FIG. 2 is a block diagram of a system 200 according to one embodiment of the present invention.

200

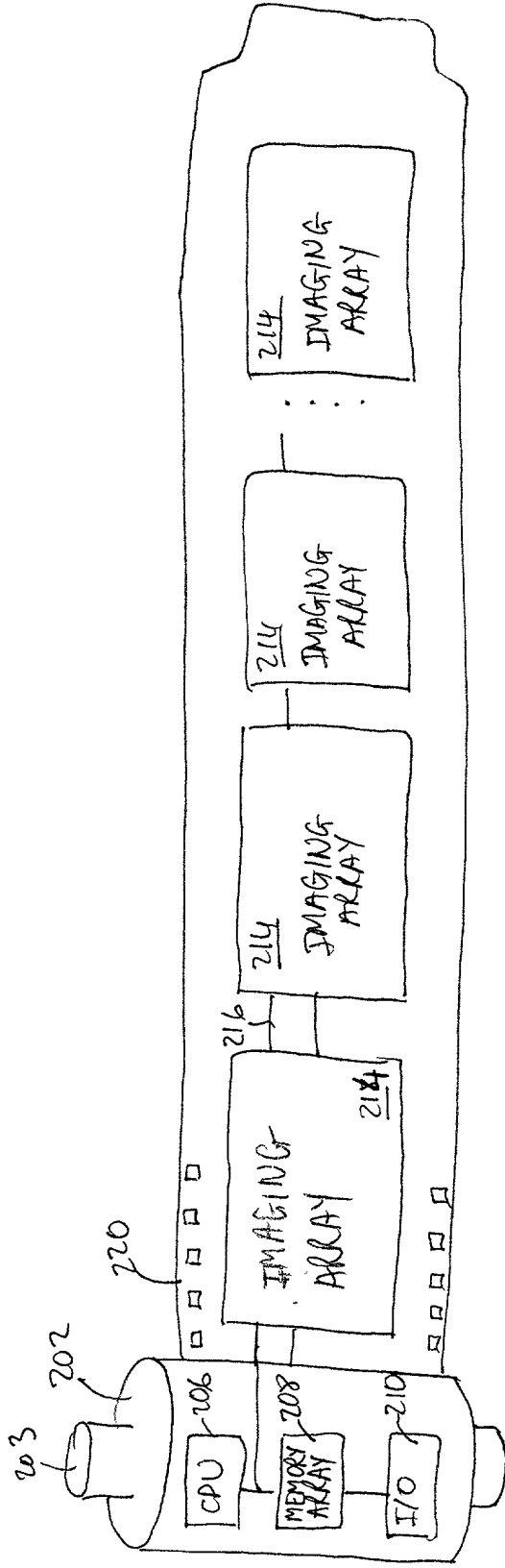


FIG. 2

FIG. 3 is a block diagram of a system 300, according to one embodiment of the present invention. The system 300 includes a processor 310, a memory 320, a network interface 330, and a user interface 340. The processor 310 is connected to the memory 320, the network interface 330, and the user interface 340. The network interface 330 is connected to a network 350. The user interface 340 is connected to the processor 310. The system 300 is shown in a perspective view.

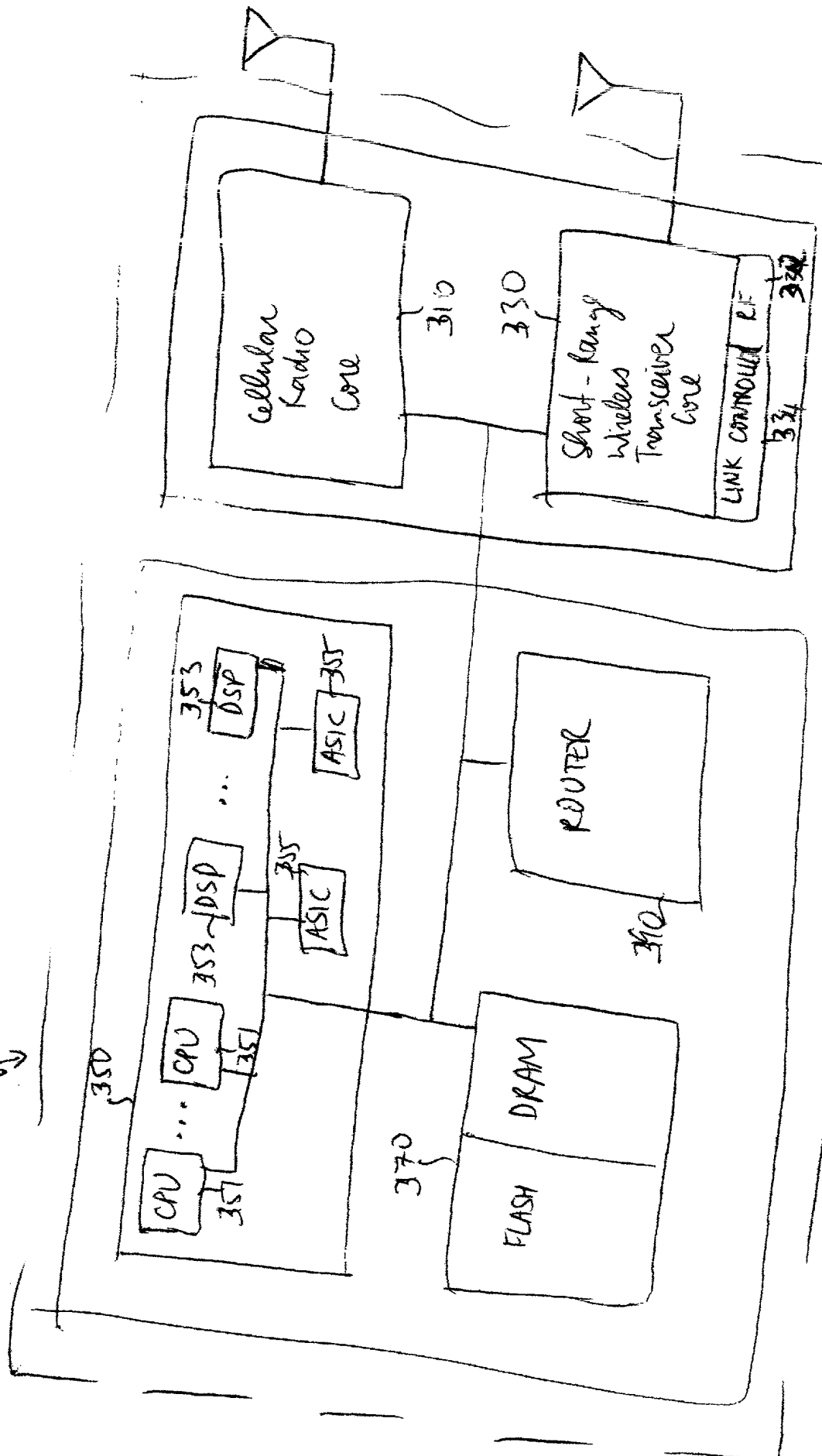


FIG. 3

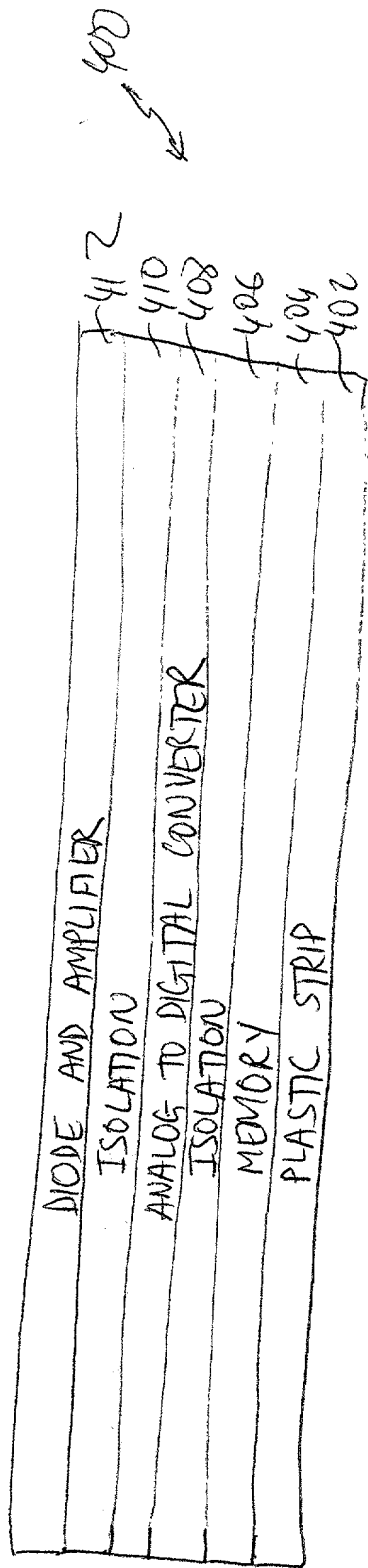


FIG. 4A

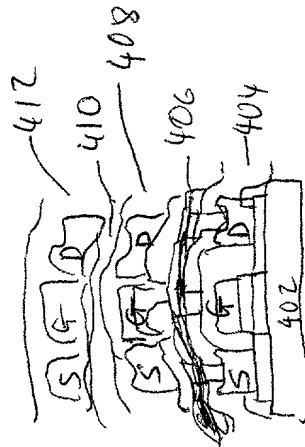


FIG. 4B